Filing Date: January 27, 2000

Title: MEMORY STRUCTURE FOR RESOLVING ADDRESSES IN A PACKET-BASED NETWORK SWITCH

REMARKS

Applicants have carefully reviewed and considered the Office Action mailed on April 7, 2010 and the references cited therein. Applicants have amended the Specification to the address matters of form and to make the Specification consistent with the drawings. Applicants have also amended claim 1 to address a matter of form. Applicants have not added any new matter by these amendments. Applicants have not canceled or added any claims. Accordingly, claims 1-60 remain pending in the application of which claims 1, 8, 13, 28, 32, 52 and 57 are independent.

Serial Number: 097492,203 Filing Date: January 27, 2000 Title: MEMORY STRUCTURE FOR RESOLVING ADDRESSES IN A PACKET-BASED NETWORK SWITCH

Claim Objections

In the Office Action, claim 1 was objected to for a formal issue. Applicants have amended claim 1 to address this concern. Accordingly, the objection to claim 1 is obviated and Applicants respectfully request that the rejection of claim 1 be withdrawn.

Claim Rejections - 35 U.S.C. § 103

Also in the Office Action, claims 1, 3-5, 6, 8-11, 13-15, 28-30, 32-34, 47-50, 52-55 and 57-60 were rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable (obvious) over U.S. Patent 6,067,300 to Baumert et al. (hereafter "Baumert") in view of U.S. Patent No 6,279,097 to Kaku, and further in view of U.S. Patent 6,151,644 to Wu. Applicants respectfully traverse this rejection.

It is well settled that in order to establish a *prima facie* showing of obviousness based on multiple references, it must be demonstrated that the references, when properly combined, disclose every element of the rejected claims. Applicants respectfully submit that even were one of skill in the art to make the proposed combination, which it is not conceded that he or she would, that combination would still fail to disclose every element of the rejected claims. While Applicants respectfully submit that the following discussion clearly demonstrates that claims 1, 3-5, 6, 8-11, 13-15, 28-30, 32-34, 47-50, 52-55 and 57-60 are not rendered obvious by Baumert, Kaku and Baumert, alone or in combination, those claims may not be obvious over Baumert, Kaku and Wu on other bases as well. Applicants reserve the right to address such bases in a future response.

Applicants begin with claim 1, which recites:

A memory structure for use with a dual-speed Ethernet device, the memory structure comprising:

an Address Resolution Table comprising a plurality of locations, each of said locations being configured to store a packet destination address, wherein the Address Resolution Table is configured to:

resolve addresses in a packet-based network switch; and use a key to index one of said locations wherein the key is a predefined portion of the packet destination address associated with said indexed location via at least an offset in address space;

a Packet Storage Table configured to:

receive a packet for storage in the packet-based network switch; and

share a preselected portion of memory with the Address Resolution Table; and

a single buffer per packet mechanism configured to receive an individual packet, wherein the single buffer per packet mechanism is configured to perform only one transmit descriptor read per said individual packet and execute a first single access in order to locate the entire packet and a second single access to

access the packet destination address at the indexed location using the key. wherein the entire packet is to be transmitted,

- wherein the memory structure implements memory arbitration for at least six types of memory accesses, and
- wherein the memory structure facilitates full-duplex, non-blocked Ethernet switch operations at wire speeds.

Claim 1 is directed to a memory structure for use with a dual-speed Ethernet device. The memory structure of claim 1 includes an Address Resolution Table that comprises a plurality of locations. In the memory structure of claim 1, each of the plurality of locations is configured to store a packet destination address. In the memory structure of claim 1, the Address Resolution Table is configured to resolve addresses in a packet-based network switch and use a key to index one of said locations wherein the key is a predefined portion of the packet destination address associated with said indexed location via at least an offset in address space.

The memory structure of claim 1 also includes a Packet Storage Table that is configured to receive a packet for storage in the packet-based network switch and share a preselected portion of memory with the Address Resolution Table. The memory structure of claim 1 further includes a single buffer per packet mechanism that is configured to receive an individual packet. The single buffer per packet mechanism is also configured to perform only one transmit descriptor read per individual packet and execute a first single access in order to locate the entire packet and a second single access to access the packet destination address at the indexed location using the key, where the entire packet is to be transmitted.

The Office Action asserts, on page 3, that the packet memory 20 of Baumert discloses the Packet Storage Table of claim 1. Specifically, the Office Action states:

A Packet Storage Table (Figures 4 and 5, packet memory 20) configured to: Receive a packet for storage in the packet-based network switch. Refer to Column 5, lines 27-28,

Share a preselected portion of memory with the Address Resolution Table. In Figure 5, packet memory 20 and address table 38 are connected to each other.

While the packet memory 20 of Baumert may be configured to receive a packet for storage in a packet-based network switch, though this is not specifically conceded, Applicants respectfully disagree that the packet memory 20 of Baumert is configured to share a preselected portion of memory with an Address Resolution Table, as is recited in claim 1. As is indicated above, the Office Action asserts that this aspect of claim 1 is disclosed by Baumert merely because "In

Filing Date: January 27, 2000

Filing Date: January 27, 2000
Title: MEMORY STRUCTURE FOR RESOLVING ADDRESSES IN A PACKET-BASED NETWORK SWITCH

Figure 5, packet memory 20 and address table 38 are connected to each other." An examination of Figure 5 of Baumert demonstrates that the packet memory 20 and the address table 38 are "connected to each other" via, at least, an address table state machine 100, a main receive state machine 92 and a packet memory output buffer 32. Applicants respectfully submit that such an arrangement does not disclose a Packet Storage Table that is configured to share a preselected portion of memory with an Address Resolution Table, as is recited in claim 1. In fact, Applicants respectfully submit that, in such an arrangement, the packet memory 20 would be completely separate from the receive controller 40 (which includes the address table 38). Additionally, the fact that the receive controller 40 is coupled with the packet memory 20 via a packet memory output buffer 32 further demonstrates that the packet memory 20 is separate from the receive controller 40 and, therefore, cannot be configured to share a preselected portion of memory with the address table 38. Neither Kaku nor Wu compensates for this deficiency of Baumert and are not cited as such. Accordingly, claim 1 in rendered obvious by Baumert, Kaku and Wu on at least this basis.

The Office Action also asserts that Baumert discloses a mechanism configured to perform only one transmit descriptor read per individual packet and execute a first single access in order to locate the entire packet and a second single access to access the packet destination address at the indexed location using the key, as recited in claim 1. However, the Office Action also conceded that Baumert fails to disclose the single packet per buffer mechanism of claim 1, where that single buffer per packet mechanism is configured to operate as such. Accordingly, the Office Action is unclear as to whether or not it is asserted that Baumert discloses the single buffer per packet mechanism of claim 1.

Nevertheless, Applicants respectfully submit that Baumert cannot disclose the aspects of claim 1 indicated in the foregoing paragraph. Because Baumert discloses storing packets across multiple buffers (See Baumert, column 5, lines 27-28), that patent cannot disclose a mechanism that is configured to perform only one transmit descriptor read per individual packet and execute a first single access in order to locate the entire packet and a second single access to access the packet destination address at the indexed location using the key, as recited in claim 1. Specifically, Baumert cannot disclose this aspect of claim 1, because performing only one transmit descriptor read per individual packet, executing a first single access in order to locate

Serial Number: 09/492,265 Filing Date: January 27, 2000

Filing Date: January 27, 2000
Title: MEMORY STRUCTURE FOR RESOLVING ADDRESSES IN A PACKET-BASED NETWORK SWITCH

the entire packet and executing a second single access to access the packet destination address at the indexed location using [a] key would not be possible for packets stored across multiple buffers. Accordingly, regardless of the assertions made in the Office Action, Baumert also fails to disclose this aspect of claim 1. Neither Kaku nor Wu are disclosed as compensating for this deficiency of Baumert. Accordingly, the Office Action has failed to establish a prima facie showing that Baumert, Kaku and Wu disclose, alone or in combination, a single buffer per packet mechanism is also configured to perform only one transmit descriptor read per individual packet and execute a first single access in order to locate the entire packet and a second single access to access the packet destination address at the indexed location using [a] key, as recited in claim 1. Thus, claim 1 is also not rendered obvious by Baumert, Kaku and Wu, alone or in combination, on at least this additional basis.

Further, the Office Action concedes that Baumert fails to disclose the "key" of claim 1. As recited in claim 1, a "key" is used to index locations of an Address Resolution Table. In the memory structure of claim 1, where the key is a predefined portion of the packet destination address associated with said indexed location via at least an offset in address space. Such an approach is illustrated in FIG. 4 of the application and descried in the application on page 8, line 1 - page 9, line 6. As described in the application on page 8, (and illustrated in FIG. 1), in one embodiment, locations in an Address Resolution Table are indexed using a key (e.g., 13 bits) that is a subset of the bits of a 48-bit MAC address via an offset 29. Regardless of the assertions made in the Office Action, Kaku does not disclose such an approach as Kaku does not disclose, describe or even mention such an offset. Kaku merely discloses indexing a table based on a subset (i.e., the 5 least-significant bits of a compressed address) of a destination address of a packet. See Kaku, column 2, lines 30-32. Regardless of the assertions made in the Office Action, Kaku does not disclose the offset recited in claim 1. Wu does not compensate for these deficiencies of Baumert and Kaku and is not cited as such. Accordingly, claim 1 is also not rendered obvious by Baumert, Kaku and Wu, alone or in combination, on at least this additional hasis

Still further, the Office Action concedes that Baumert fails to disclose the single packet per buffer mechanism recited in claim 1 and, instead, cites Wu as disclosing this aspect of claim 1. However, as noted above, the Office Action asserted that Baumert allegedly discloses a Title: MEMORY STRUCTURE FOR RESOLVING ADDRESSES IN A PACKET-BASED NETWORK SWITCH

mechanism that functions in like manner as the "single packet per buffer" mechanism of claim 1. As discussed above, Baumert cannot, in fact, disclose such a mechanism. As also discussed above, the Office Action fails to establish that Wu compensates for the deficiencies of Baumert regarding the single packet per buffer mechanism recited in claim 1. Kaku also does not compensate for the deficiencies of Baumert and Wu and is not cited as such. Accordingly, Baumert, Kaku and Wu, alone or in combination, further fail render claim 1 obvious with respect to the single packet per buffer mechanism of that claim.

Based on the foregoing, claim 1 is not rendered obvious by Baumert, Kaku and Wu for at at least the reasons discussed above. Accordingly, Applicants respectfully request that the rejection of claim 1 be withdrawn.

Without addressing the remarks made in the Office Action with respect to independent claims 8, 13, 28, 32, 52 and 57, Applicants note that each of those independent claims includes one or more similar limitations as the limitations discussed above with respect to claim 1. Accordingly, independent claims 8, 13, 28, 32, 52 and 57 are not rendered obvious by Baumert, Kaku and Wu for reasons similar to those discussed above with respect to claim 1. Applicants, therefore, respectfully request that the rejection of independent claims 8, 13, 28, 32, 52 and 57 also be withdrawn

Without addressing the remarks made in the Office Action with respect to dependent claims 3-5, 6, 9-11, 14, 15, 29, 30, 33, 34, 47-50, 53-55 and 58-60, which are not conceded, Applicants note that these claims are not rendered obvious by virtue of their respective dependencies on independent claims 1, 8, 13, 28, 32, 52 and 57. Accordingly, Applicants respectfully request that the rejection of claims 3-5, 6, 9-11, 14, 15, 29, 30, 33, 34, 47-50, 53-55 and 58-60 be withdrawn.

Further in the Office Action, dependent claims 2, 7, 12, 16-27, 31, 35-46, 51 and 56 were rejected under 35 U.S.C. § 103(a) as being allegedly obvious over Baumert, Kaku and Wu in combination with one or more of U.S. Patent 6,021,132 to Muller et al. (hereafter "Muller"); U.S. Patent 5,765,036 to Lim; U.S. Patent 6, 088,793 to Liu et al. (hereafter "Liu"); and U.S. Patent 5,940,275 to Soumiya et al. (hereafter "Soumiya").

Without addressing the remarks made in the Office Action with respect to claims 2, 7, 12, 16-27, 31, 35-46, 51 and 56, which are not conceded, Applicants note that these claims each

Serial Number: 09/492,265 Dkt: 0063-022004/BU1279
Filing Date: January 27, 2000
Title: MEMORY STRUCTURE FOR RESOLVING ADDRESSES IN A PACKET-BASED NETWORK SWITCH

depend from one of the independent claims discussed above. Applicants also note that none of Muller, Lim, Liu and Soumiya compensate for the deficiencies of Baumert, Kaku and Wu discussed above. Accordingly, independent claims 1, 8, 13, 28, 32, 52 and 57 are not rendered obvious by Baumert, Kaku, Wu, Muller, Lim, Liu and Soumiya, alone or in combination. Therefore, by virtue of claim dependency, dependent claims 2, 7, 12, 16-27, 31, 35-46, 51 and 56 are also not rendered obvious by Baumert, Kaku, Wu, Muller, Lim, Liu and Soumiya, alone or in combination. Applicants respectfully request that the rejections of dependent claims 2, 7, 12, 16-27, 31, 35-46, 51 and 56 be withdrawn.

Conclusion

Applicants believe that all the claims pending in the application are in condition for allowance. The Examiner may telephone Applicant's attorney (360-930-3533) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-3521.

Respectfully submitted,

Reg. No. 47,495

Brake Hughes Bellermann LLP Customer No.: 57246

Date June 3, 2010 By: /Paul W. Churilla – Reg. No. 47,495/
Paul W. Churilla